International Microsystems IM-1010 Programmer repair

3-30-2020

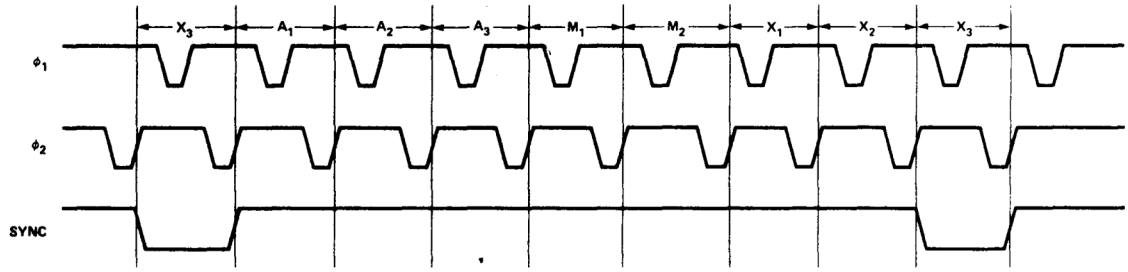
Loking for remote Terminal activity, assuming display is dead. Run TeraTerm as Administrator. No Null Modem. Nothing at all – display or TeraTerm

Voltages to CPU: Leftmost end (Brown) Ground. +5 (Black), -5 (White), +11.6 (Black), N/C, -10 (White).
Voltages to UART bord: Ground (Brown), +5, N/C, 11.6, -12.2, -10.
Voltages to Display: Ground (Brown) 5, +11.6, -10,
Voltages to RAM board with module removed: OK
Looks like the high Power Supply voltages only go to the programming module (+50, +34, ++92, +54, 70VAC, 36VAC, &+15 from remote power supply).

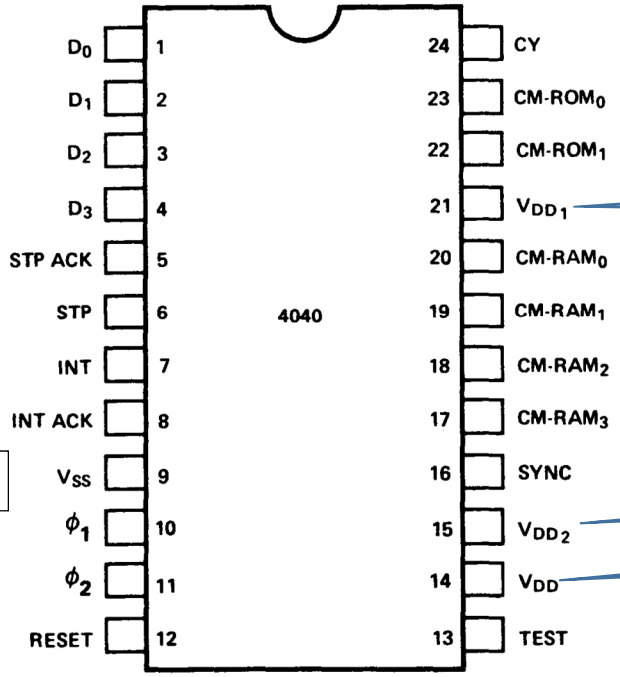
Note that the memory board used uPD411AC 4kbit x 1 chips – can't find data sheet on line.

3-31-2020
Had downloaded complete Intel 4040 manual. Excerpt from one page shows astounding limits of 4 bits and amazing performance in spite of this limitation:

"All MCS-40 inter-element communication transpires over a four bit data bus (00-03), 03 being the most significant bus bit. The data bus transfers information from the processor to the memory and I/O elements such as instruction addresses, operand addresses, operands, and I/O data. The processor receives instructions; operands, and I/O data back from the other elements. All traffic on the bus is contained within one instruction cycle for one cycle instructions. The instruction cycle is subdivided into equal time segments. Each segment is equ ivalent to one system clock period. Information on the data bus is altered from segment to segment The first three time segments present a twelve bit (three groups of four bits) instruction address to the memory, least significant nibble first. The fourth and fifth segments provide the 8 bit instruction sequentially placed on the data bus by program memory. The sixth segment is utilized for instruction decode. The remaining two segments are used for program execution. Operands and I/O data can be found on the data bus during this time, depending on the instruction being executed."



VDD = -15V



VDD1 Timing = -15V

VSS most Positive

VDD2 = Buffers

VDD = -15V

Pin Description

Pin No.	Designation	Description of Function
1-4	D_0-D_3	Bidirectional data bus. All address and data communication between the processor and the RAM and ROM chips is handled by way of these 4 lines.
5	STPA	STOP ACKNOWLEDGE output. This signal acknowledges that the processor has entered the stop mode. Output is "open drain" requiring pull-down resistor to V_{DD}.
6	STP	STOP input signal. A logic "1" level at this input causes the processor to enter the STOP mode.
7	INT	INTERRUPT input signal. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.
8	INTA	INTERRUPT ACKNOWLEDGE output. This signal acknowledges receipt of an INTERRUPT command and prevents additional INTERRUPTs from entering the processor. INTERRUPT ACKNOWLEDGE remains active until cleared by the new BRANCH BACK and SRC (BBS) instruction. The output is "open drain", requiring a pull-down resistor to V_{DD}.
9	V_{SS}	Circuit GND potential – most positive supply voltage.
10-11	ϕ_1-ϕ_2	Non-overlapping clock signals which determine processor timing.
12	RESET	RESET input. A "1" level applied to this pin clears all flag and status flip-flops and forces the program counter to 0. To completely clear all of the address and index registers, RESET must be applied for 96 clock cycles(12machine cycles).
13	TEST	TEST input. The logical state of this input can be examined with the JCN instruction.
14	V_{DD}	Main supply voltage to the processor. Value must be V_{SS} -15.0V ±5%.
15	V_{DD2}	Supply voltage for output buffers. May be varied depending on interface conditions.
16	SYNC	SYNC output. Synchronization signal generated by the processor and sent to ROM and RAM chips. Indicates beginning of instruction cycle.
17-20	CM-RAM_0-CM-RAM_3	CM-RAM outputs. These outputs act as bank select signals for the 4002 RAM chips in the system.
21	V_{DD1}	Supply voltage for timing circuit. Value must be V_{SS} -15.0V ±5%. Allows low power standby operation. Only SYNC will be generated when this pin is the only active V_{DD}.
22-23	CM-ROM_0-CM-ROM_1	CM-ROM outputs. These outputs act as bank select signals for the ROM chips in the system.
24	CY	CARRY output buffer. The state of the CY flip-flop is presented at this output and is updated at X_1. The output is "open drain" requiring a pull-down resistor to V_{DD}.

Basic Circuit Timing

The basic system timing for the 4040 is identical to that used for the 4004, as shown in the following figure. Two non-overlapping clock signals, ϕ_1 and ϕ_2, are used to define the basic timing. The start of an instruction cycle is indicated by the SYNC signal, which is generated by the processor and sent to the various ROM and RAM or peripheral chips in the system. An instruction cycle consists of the following operations:

1. The 12 bit content of the program counter is sent out to the ROM chips in three 4 bit groups during A_1, A_2, A_3.
2. The 8 bit instruction or data from the addressed ROM location is received by the processor at M_1 and M_2 at which time the instruction is decoded.
3. Instruction execution occurs during X_1, X_2, and X_3. Data or address information may be sent to output ports or RAM chips; data may be received from input ports or RAM chips; or data may be operated on within the processor.

The data bus contents at the various times of the instruction cycle are defined just as for the 4004 with the exception of the data at X_1 and the carry output during X_3 of a No-Op instruction. The 4040 outputs the contents of the accumulator at X_1 for program debugging purposes, whereas the 4004 simply copies the data which it received at M_2. The data

3-31-2020
Found Pin 9 at +5V and therefore could not use as scope ground. Find Ground on J5 pin 9 (next to last on right), the 10 pin test connector at the top of the board. Connected scope ground here.

Find no activity on 4040 pins 10, 11, 16 all at +5V static. Pin 12 (reset) at +1.8V.

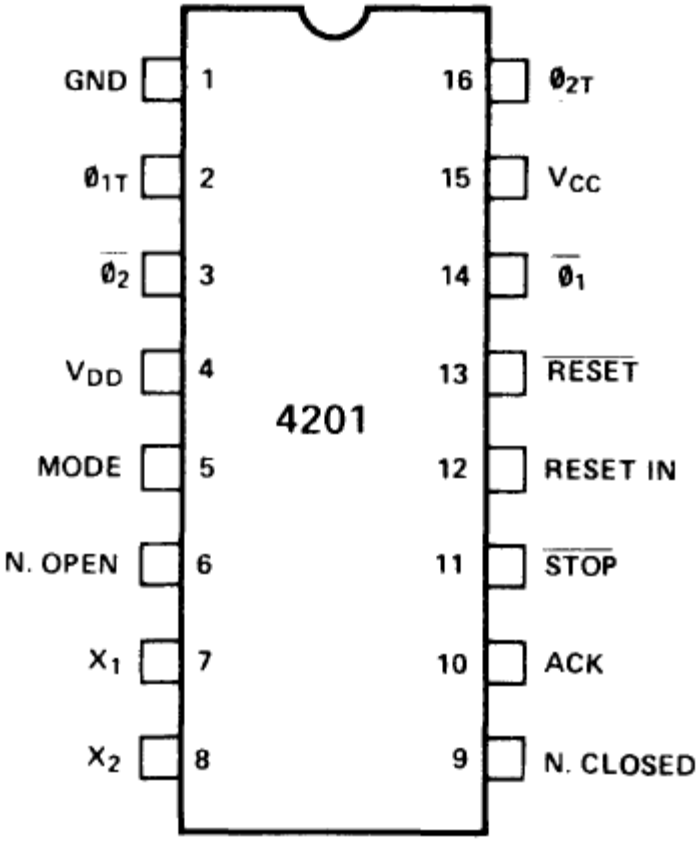
Went to 4201 timing chip on page 67 of MCS40 book. . Pin 4 (VDD) =-10. Pin 1 (GND) = 0. Pin 15 (VCC) = +5. Oscillator inputs in pins 7 & 9 3V & 1/2V static. Pin 12 (Reset in) = +1.8V static. Reset button does change voltage slightly.

Removed display/kbd interface board to test continuity of "RESET" switch. It is flakey – drops to 15 Ohms across switch sometimes, but not always. Reset In is also on Pin 5 of J5 (test connector). On Pin 5, Reset In varies from +1.16 to +0.94 when depressed. Display/KBD schematic is screwed up, but although RESET (IN) key is separate from matrix decoder inputs, seems to go to resistor network (10K) through 100 Ohm (where is it?) to -10V source. PIN 5 of test connector indeed goes to one side of reset switch, other side of switch measures 200K when open. PIN 7 of test connctor is supposed to be -10V supply,; measure from pin 7 to -10: 100k when switch open, 50k when closed. Using scope on single-sweep, find ~200uSec rise-fall time from 1.14 to 1.0 Volts on PIN 12 of 4201. There is -10V on upper side of RESET switch – where does the +1 come from? Display schematic is ambiguous. Test CR1, which goes to +5 Volts. Diode seems OK. Measured C25 (nominally .1 uF); measured .086uF.

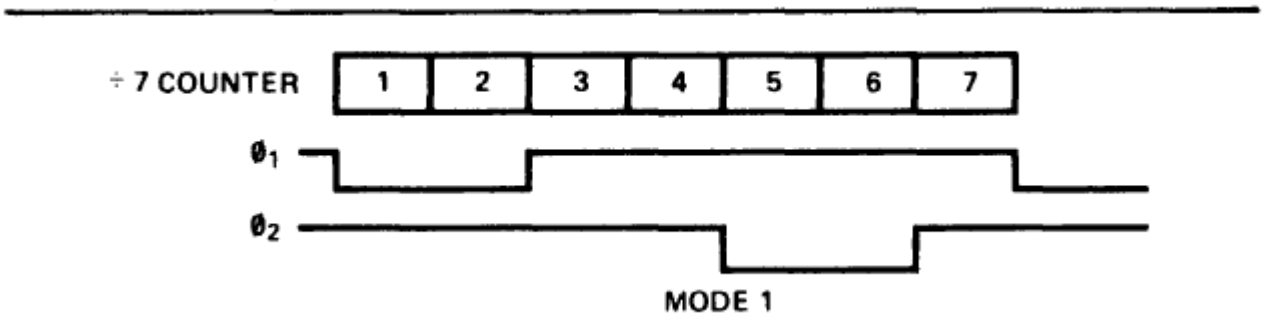
4-1-20
Removed all conectors and pulled CPU board to trace the RESET IN components. Drew partial schematic – it does match the CPU-32 schematic, although component names are not the same. RESET IN goes through a 470 Ohm resistor then to the + side or CR1 which then goes to +5 Volts; also to 100K R5 which then goes to ground. Then to a "104" capacitor C5 which then goes to -10. Removed the 4201 clock chip.

4-2-20
Re-attached the 4 cables to the CPU (loosely) but left the 4201 out. Powered up and measured RESET IN" between pins 5 and 9 of the test connector, J5. Button is still flakey (1 of 5 hits works) but captured one trace indicating the circuit is doing what I think it is supposed to: normally 0 Volts, drops to -5V with a RC time of 5-10 mSec. (but occasionally scope triggers on nothing detectable?)

With 4201 inserted, get same very small pulse as before: from +1.18 to +1 Volt when pushed.



YIKES: checking the signals on the 4201 pins, happened to touch pins 1-3 or 3-6 with a finger – get signals and even oscillation! E.g., on pin 14 (phi1/), got 30 mSec negative going pulses. Better yet, moving the 16 pin clip, get steady oscillation in some positions. 30 mSec negative going (from +5 to 0) pulses each 100 mSec. Pin 14 and sometimes 3 are only pins with live signal – not 2, or 16. But 3 & 14 are the only ones used by the 4040. Stranger: even coming close to the clip induces output on pins 3 & 14. Toughing XTAL input pins (8 or 7) or leaving test lead flying also induces outputs – perhaps the XTAL is dead? No signal found on pins 7 & 8 and no direct Oscillator output except the phase 1 & 2. If flying lead causes oscillation at 120 Hz, that is 8.8 mSec; divide by 7 or 8 is roughly 60 mSec. Touching C8 or C9 or crystal causes same steady phase 1 & 2 outputs. MODE pin 5 is at +5V = VSS = VCC so Mode=1.



The ouputs, when they are there, do look pretty much like this.

Replaced the XTAL with a 3.6MHz – power up – no oscillations unless the leads are touched.

With the flakey reset and lack of oscillation (and the dead TTL PHI1-PHI2 outputs), best guess is dead 4201. Some parts listed on line at ~$40, but have to declare finis.